

# CLC5654

## Very High Speed, Low Cost, Quad Operational Amplifier

### General Description

The CLC5654 is a quad, current feedback operational amplifier that is perfect for many cost sensitive applications that require high performance. This device also offers excellent economy in board space and power, consuming only 5mA per amplifier while providing 70mA of output current capability. Applications requiring significant density of high speed devices such as video routers, matrix switches and high order active filters will benefit from the configuration of the CLC5654 and the low channel-to-channel crosstalk of 70dB at 5MHz.

The CLC5654 provides excellent performance for video applications. Differential gain and phase of 0.03% and 0.03° makes this device well suited for many professional composite video systems, but consumer applications will also be able to take advantage of these features due to the device's low cost. The CLC5654 offers superior dynamic performance with a small signal bandwidth of 450MHz and slew rate of 2000V/ $\mu$ s. These attributes are well suited for many component video applications such as driving RGB signals down significant lengths of cable. These and many other applications can also take advantage of the 0.1dB flatness to 40MHz.

Combining wide bandwidth with low cost makes the CLC5654 an attractive option for active filters. SAW filters are often used in IF filters in the 10's of MHz range, but higher order filters designed around a quad operational amplifier may offer an economical alternative to the typical SAW approach and offer greater freedom in the selection of filter parameters. National Semiconductor's Comlinear Products Group has published a wide array of literature on active filters and a list of these publications can be found on the last page of this datasheet.

### Features

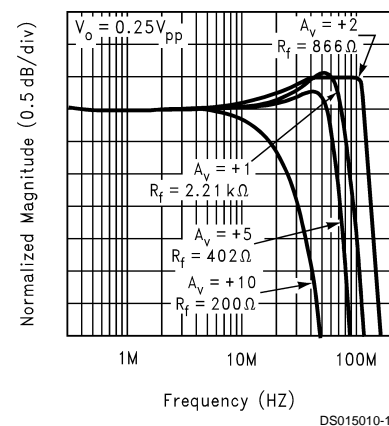
- 450MHz small signal bandwidth

- 2000 V/ $\mu$ s slew rate
- 5mA/channel supply current
- -71/-82dBc HD2/HD3 (5MHz)
- 0.03%, 0.03° differential gain, phase
- 70mA output current
- 12ns settling to 0.1%

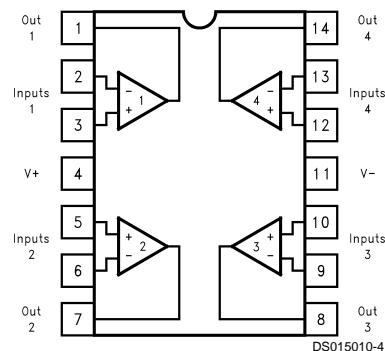
### Applications

- High performance RGB video
- Video switchers & routers
- Video line driver
- Active filters
- IF amplifier
- Twisted pair driver/receiver

Non-Inverting Frequency Response

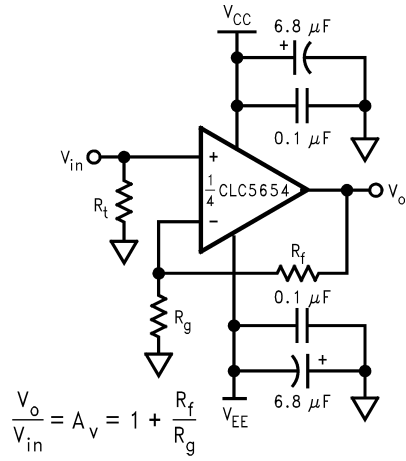


### Connection Diagram



Pinout  
DIP & SOIC

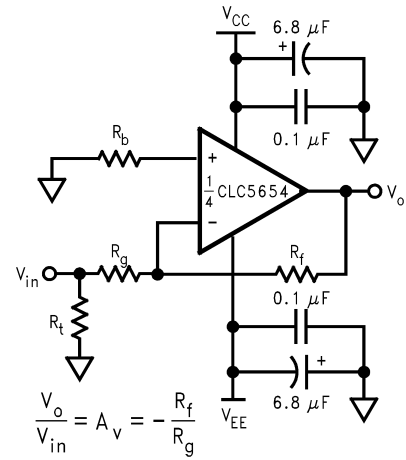
## Typical Configurations



$$\frac{V_o}{V_{in}} = A_v = 1 + \frac{R_f}{R_g}$$

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**Non-Inverting Gain**



$$\frac{V_o}{V_{in}} = A_v = -\frac{R_f}{R_g}$$

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Note:  $R_t$  provides DC bias for the non-inverting input. Select  $R_t$  to yield desired  $R_{in} = R_t \parallel R_g$ .

**Inverting Gain**

## Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-pin plastic DIP	-40°C to +85°C	CLC5654IN	CLC5654IN	N14A
14-pin plastic SOIC	-40°C to +85°C	CLC5654IM	CLC5654IM	M14A
		CLC5654IMX		

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}-V_{EE}$ )	+14V
Output Current	95mA
Common-Mode Input Voltage	$V_{EE}$ to $V_{CC}$
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C

Lead Temperature (soldering 10 sec)

+300°C

**Operating Ratings**

Thermal Resistance		
Package	( $\theta_{JC}$ )	( $\theta_{JA}$ )
MDIP	60°C/W	110°C/W
SOIC	55°C/W	125°C/W

**Electrical Characteristics**(A<sub>V</sub> = +2, R<sub>f</sub> = 866Ω, R<sub>L</sub> = 100Ω, V<sub>S</sub> = ±5V, unless specified)

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)		Units
Ambient Temperature		CLC5654IN/IM	+25°C	+25°C	-40 to 85°	
<b>Frequency Domain Response</b>						
	-3dB Bandwidth	A <sub>V</sub> = 1	450	-	-	MHz
		V <sub>O</sub> < 0.5V <sub>PP</sub>	350	-	-	MHz
		V <sub>O</sub> < 5V <sub>PP</sub>	100	-	-	MHz
	-0.1dB Bandwidth		40	-	-	MHz
	Differential Gain	NTSC, R <sub>L</sub> = 150Ω	0.03			dB
	Differential Phase	NTSC, R <sub>L</sub> = 150Ω	0.03			dB
<b>Time Domain Response</b>						
	Rise and Fall Time	0.5V Step	1.2	-	-	ns
		5V Step	2.7	-	-	ns
	Settling Time to 0.1%	2V Step	12	-	-	ns
	Overshoot	0.5V Step	7	-	-	%
	Slew Rate		2000	-	-	V/μs
<b>Distortion And Noise Response</b>						
	2nd Harmonic Distortion	2V <sub>PP</sub> , 5MHz	-71	-	-	dBc
	3rd Harmonic Distortion	2V <sub>PP</sub> , 5MHz	-82	-	-	dBc
	Equivalent Input Noise					
	Voltage (e <sub>ni</sub> )	>1MHz	3.3	-	-	nV/√Hz
	Non-Inverting Current (i <sub>bn</sub> )	>1MHz	2.5	-	-	pA/√Hz
	Inverting Current (i <sub>bi</sub> )	>1MHz	12	-	-	pA/√Hz
	Crosstalk (Input inferred)	10MHz	76	-	-	dB
<b>Static, DC Performance</b>						
	Input Offset Voltage (Note 3)		2.5	6	11	mV
	Average Drift		18	-	55	μV/°C
	Input Bias Current (Non-Inverting)(Note 3)		6	15	28	μA
	Average Drift		40	-	160	nA/°C
	Input Bias Current (Inverting) (Note 3)		5	12	20	μA
	Average Drift		25	-	120	nA/°C
	Power Supply Rejection Ratio	DC	55	47	45	dB
	Common Mode Rejection Ratio	DC	50	45	43	dB
	Supply Current (per channel) (Note 3)	R <sub>L</sub> = ∞	5	6.7	7	mA

## Electrical Characteristics (Continued)

( $A_V = +2$ ,  $R_f = 866\Omega$ ,  $R_L = 100\Omega$ ,  $V_S = \pm 5V$ , unless specified)

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)		Units
<b>Miscellaneous Performance</b>						
	Input Resistance (Non-Inverting)		1	0.5	0.25	M $\Omega$
	Input Capacitance (Non-Inverting)		1	2	2	pF
	Common Mode Input Range		$\pm 2.2$	$\pm 2.0$	$\pm 1.4$	V
	Output Voltage Range	$R_L = 150\Omega$	$\pm 2.6$	$\pm 2.5$	$\pm 2.3$	V
	Output Current		70	50	40	mA
	Output Resistance, Closed Loop	DC	0.2	0.3	0.6	m $\Omega$

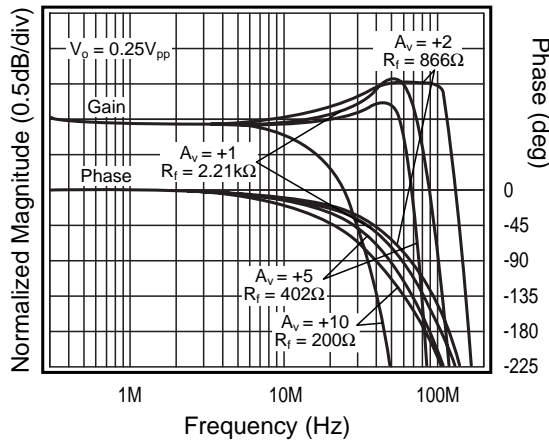
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

**Note 3:** AJ-level: spec. is 100% tested at +25°C.

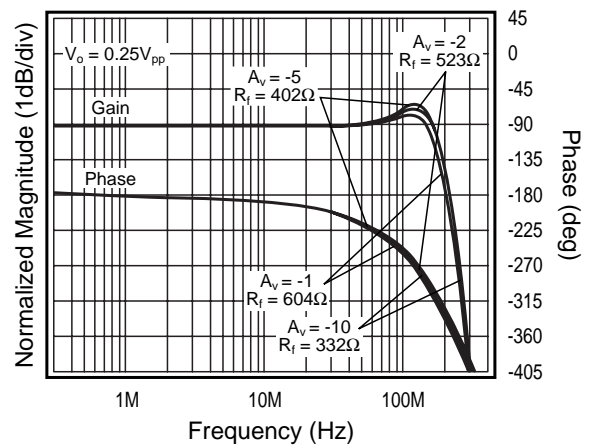
## Typical Performance Characteristics ( $A_V = +2$ , $R_f = 866\Omega$ , $R_L = 100\Omega$ , $V_S = \pm 5V$ , unless specified)

### Non-Inverting Frequency Response



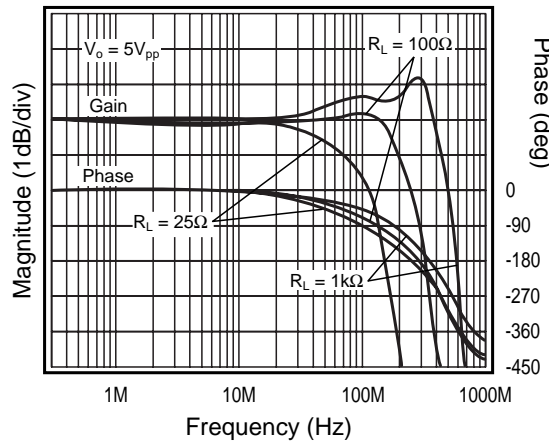
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### Inverting Frequency Response



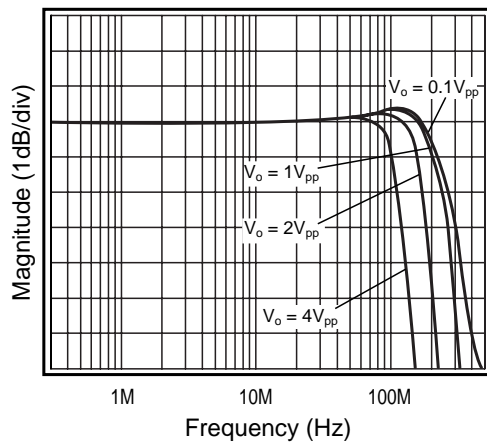
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### Frequency Response vs. $R_L$



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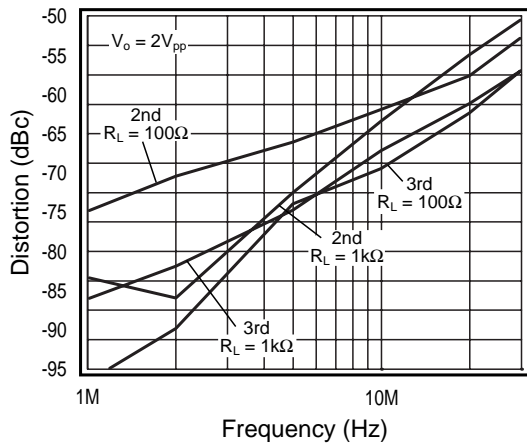
### Frequency Response vs. $V_o$



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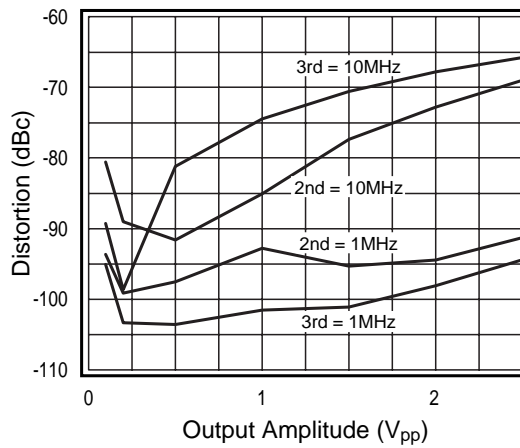
**Typical Performance Characteristics** ( $A_V = +2$ ,  $R_f = 866\Omega$ ,  $R_L = 100\Omega$ ,  $V_s = \pm 5V$ , unless specified) (Continued)

**2nd & 3rd Harmonic Distortion**



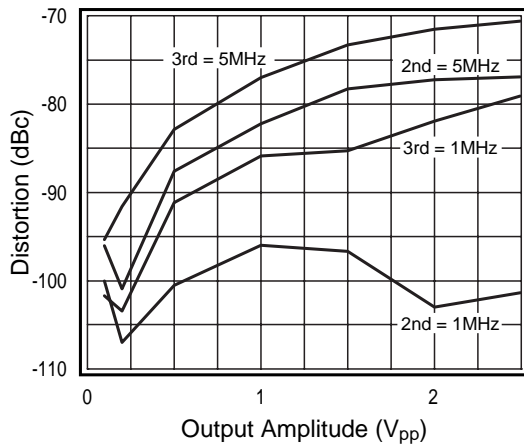
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**2nd & 3rd Harmonic Distortion,  $R_L = 1k\Omega$**



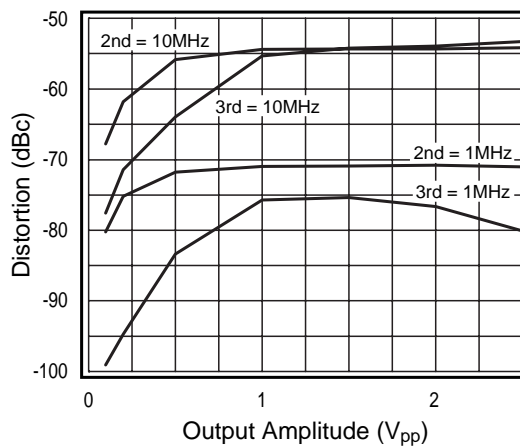
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**2nd & 3rd Harmonic Distortion,  $R_L = 100\Omega$**



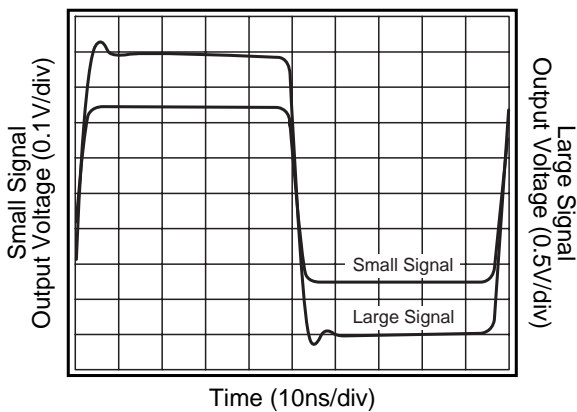
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**2nd & 3rd Harmonic Distortion,  $R_L = 25\Omega$**



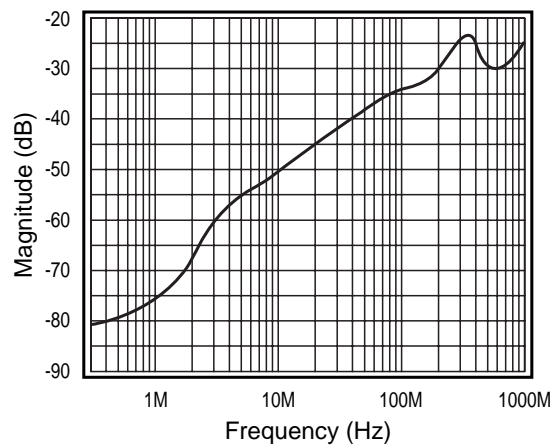
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**Large & Small Signal Pulse Response**



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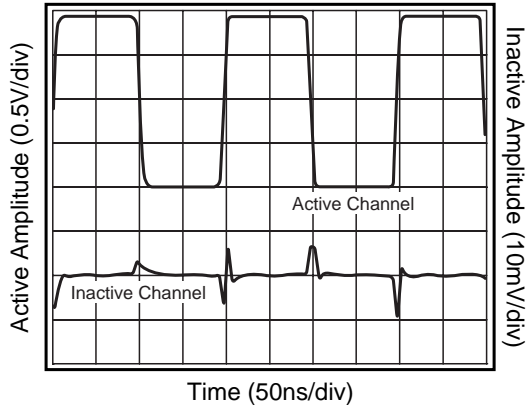
**All Hostile Crosstalk**



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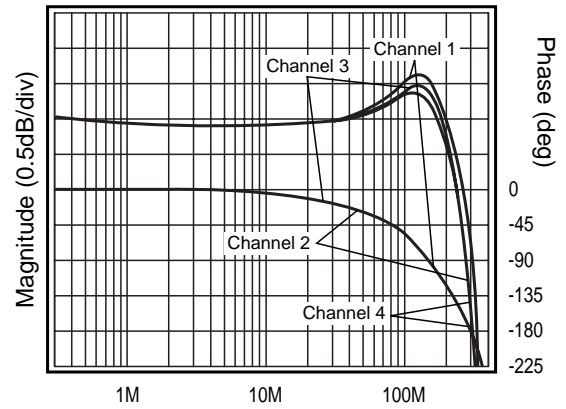
**Typical Performance Characteristics** ( $A_V = +2$ ,  $R_f = 866\Omega$ ,  $R_L = 100\Omega$ ,  $V_s = \pm 5V$ , unless specified) (Continued)

**Most Susceptible Channel Pulse Coupling**



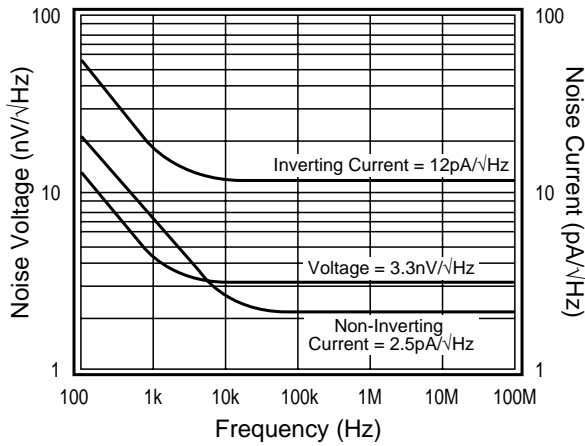
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**Channel to Channel Gain Matching**



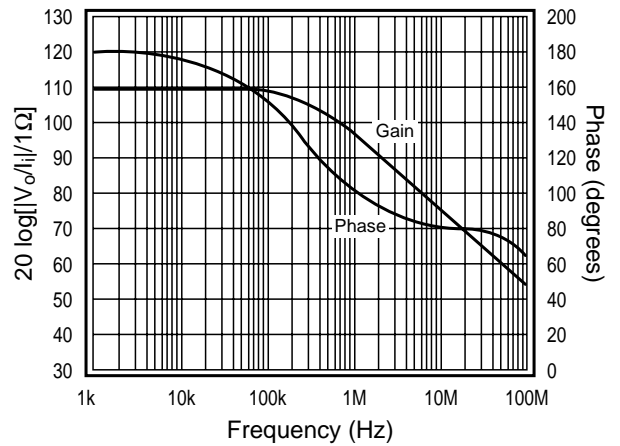
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**Equivalent Input Noise**



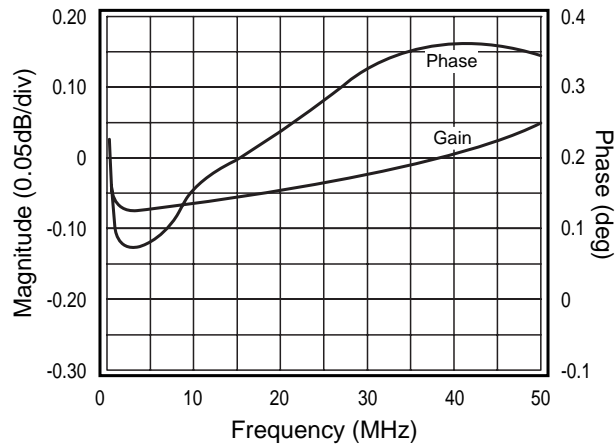
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**Open-Loop Transimpedance Gain, Z(s)**



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**Gain Flatness & Linear Phase**



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## Application Division

### Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with  $R_f$
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_i} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \quad (1)$$

where:

$A_v$  is the closed loop DC voltage gain

$R_f$  is the feedback resistor

$Z(j\omega)$  is the open loop transimpedance gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the  $-3\text{dB}$  corner frequency, the interaction between  $R_f$  and  $Z(j\omega)$  dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing  $R_f$  has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot

- Affects frequency response phase linearity

### Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5654 (CLC730024-DIP, CLC730031-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization. General layout and supply bypassing play major roles in high frequency layout:

- Include  $6.8\mu\text{F}$  tantalum and  $0.1\mu\text{F}$  ceramic capacitors on both supplies.
- Place the  $6.8\mu\text{F}$  capacitors within 0.75 inches of the power pins.
- Place the  $0.1\mu\text{F}$  capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

### Active Filter Application Notes

OA-21 Simplified Component Pre-Distortion for High Speed Active Filters

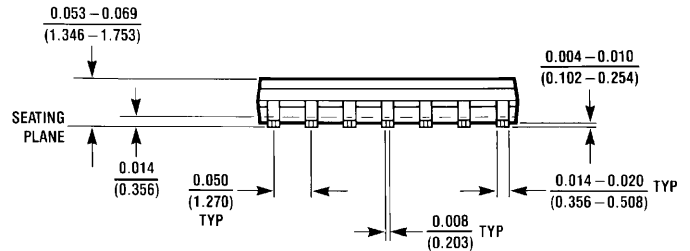
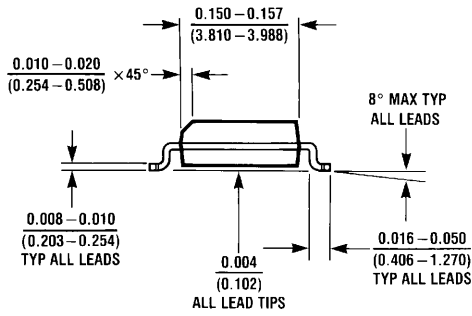
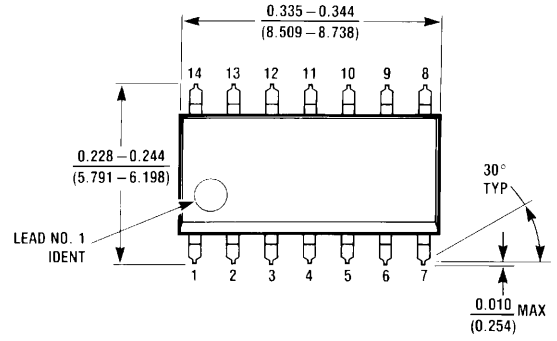
OA-26 Designing High-Speed Active Filters

OA-27 Low-Sensitivity, Lowpass Filter Design

OA-28 Low-Sensitivity, Bandpass Filter Design with Tuning Method

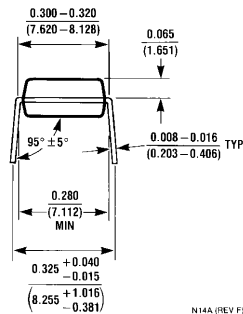
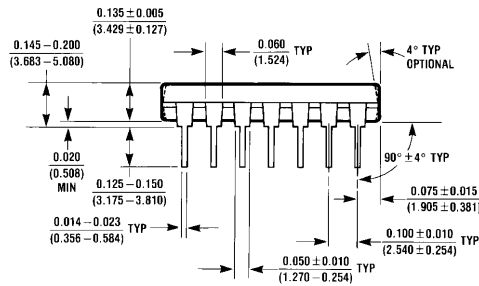
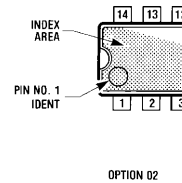
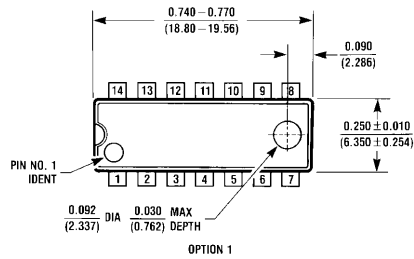
OA-29 Low-Sensitivity, Highpass Filter Design with Parasitic Compensation

**Physical Dimensions** inches (millimeters) unless otherwise noted



M14A (REV H)

**14-Pin SOIC**  
**NS Package Number M14A**



N14A (REV F)

**14-Pin MDIP**  
**NS Package Number N14A**



## Notes

### LIFE SUPPORT POLICY

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